International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970)
Volume-3 Number-1 Issue-8 March-2013

A Multi Maximal Length Multi Time Period Pseudorandom Bit Sequence (PRBS) Generator

Aritra Sinha[1], Sunit Kumar Sen[2]
M. Tech Scholar, Dept. of Applied Physics, UCSTA, University of Calcutta, India[1]
Professor, Dept. of Applied Physics, UCSTA, University of Calcutta, India[2]

Abstract

A novel method of generating a pseudorandom binary sequence (PRBS) test signal generator is presented. A traditional PRBS generator uses a linear feedback shift register (LFSR) which generates a single maximum length sequence pattern having a fixed period. In this paper, three shift registers with feedback connections are employed in which the preset inputs of the shift registers are changed only on completion of their length sequences. These preset inputs are changed by employing a counter, the time period of the clock of which equals the time of the length sequence. Thus, by employing a limited number of shift registers, a considerable increase in the length sequence is possible. This longer length sequence would enable to detect malfunction in a better way associated with specific data patterns.

Keywords

PRBS, maximal length binary sequence, bit error rate, word synchronization, system identification.

1. Introduction

PRBS signals are deterministic binary sequences having properties resembling those of a band limited white noise. A PRBS signal has low correlation with its delayed version. Again, PRBS signals are balanced. Because of these properties, PRBS signals find wide use in cryptography, spread spectrum communication systems etc.

A very common and convenient method for generation of a PRBS signal is to employ synchronous LFSRs. Figure 1 shows an n-stage LFSR having n taps t1, t2,…, tn. Each of these taps has gains of either 0 or 1. The feedback path from the nth tap is mandatory. This is summed, in mod-2 format, with the values of the registers having unity taps (from t1, t2,…, tn).

In the case of a 6 stage (n=6) LFSR, if the taps are taken from t2 and t6, then the set is designated as [6, 2]. For higher performance, a 2-tap system is advisable to be used rather than more than two taps and multiple XOR gates, as it introduces considerable delays. For a practical LFSR, a two tap system is used.

Properties of PRBS are dependent on n, the number of LFSR stages and the tap configuration. A particular tap configuration gives rise to a specific PRBS. Some applications, like BER testing of I/O channels, require many PRBS strings with varied periods. This helps in evaluating the channel for data pattern dependencies and various degrees of DC unbalance. Such application areas demand many PRBS strings for dependable testing of the said channels. Digital test signals like PRBS has applications in measurement of error rates and in the display of eye diagrams. The ultimate eye pattern obtained is the sum of the individual waveform segment shapes and these are functions of sequences of symbols.

Again, the amount of inter symbol interference (ISI) present at any instant at the regenerator is usually a function of the particular symbol pattern that occurred just prior to that instant. It is known that some particular transmitted symbol sequences give rise to more ISI at the regenerator. It is thus advisable to use test signals to have all possible symbol sequence pattern to properly evaluate the performance characteristics of transmitted signals.

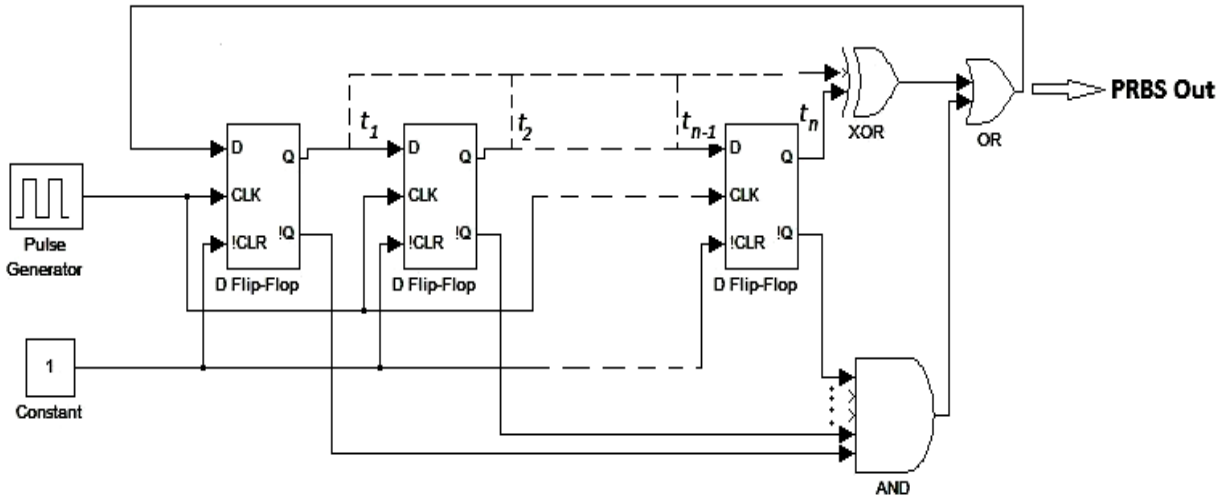

Figure 1: The general form of an LFSR

A Chow et al [**1**] proposed an alternative PRBS generator that used coupled asynchronous FIFO rings. This allowed the designed circuit to generate different maximal length PRBS patterns. Their design is less complex and offered a higher throughput. An asynchronous-to-clocked interface would enable the circuit to work synchronously. It employs an inherent pipelining technique which eliminates the need to have large feedback logic overhead in configurations with many taps. It allowed the designed PRBS to produce different patterns of different periods unlike a traditional PRBS which produces a single maximal length pattern with a fixed period. S Kim [**2**] et al proposed a 45Gb/s PRBS generator and checker that was designed, fabricated and tested using SIGe BICMOS technology. A host of other research workers also worked in this field of PRBS generation, testing and bit error detection [**3-7**]. In [**8**], a PRBS generator has been designed which gives parallel outputs. This is realized by a simple matrix multiplication technique and recursive formula. The parallel architecture improves the throughput by 2, 4 and 6 times compared with the existing scheme based on a single output.

The present paper describes a 3-stage shift register configuration in feedback mode to generate multi maximal length sequences having different time periods. A simple 3-stage LFSR has the capacity to generate a single PRBS of maximal length sequence seven only. In the present hardware design, the feedback tap positions are automatically switched giving rise to a sequential length of fourteen. In this case, the preset of the three flip flops are assigned some arbitrary value. In the subsequent experimental set up, a combination of automatic shifting of feedback connection at the end of current sequence length and changing the preset values of the flip flops would enable the PRBS output length to be enhanced to one hundred twelve. This length can further be extended to two hundred twenty four by employing an up-down counter. Malfunctioning associated with particular data patterns can more effectively be detected with longer length sequences [**9**].

2. Generalized relation for output PRBS length sequence

For a three stage LFSR, there are two possible feedback taps t_1 and t_2 with t_3. Let the sequence lengths for feedback taps t_1 and t_2 with t_3 be X_1 and X_2 respectively. In the auto switching mode as it is here, when the feedback tap was in t_1, PRBS output was obtained with a sequence length X_1 at which time it is automatically switched over to feedback path t_2. Thus, PRBS output is continued to be obtained with a sequence length X_2. Hence, when in the auto switching mode, the ultimate length of PRBS output would be

Length = $X_1 + X_2$

For a n bit shift register,

$$\text{Length} = X_1 + X_2 + \ldots\ldots\ldots\ldots + X_{n-1} \qquad (1)$$

$$= \sum_{i=1}^{n-1} X_i$$

This output PRBS length sequence is obtained for fixed preset values of the shift registers. If after completion of this, the preset values are automatically changed, the total number of preset combinations would be 2^n for an n stage LFSR and in that case the output length sequence would be as per equation (2).

$$\text{Length} = 2^n . \sum_{i=1}^{n-1} X_i \qquad (2)$$

For the present case of a three stage LFSR, n = 3 and the output length sequence will be = 2^3. (7+7) = 112.

3. Circuit Design

The block schematic of the circuit which provides a PRBS of length sequence fourteen is shown in figure 2. There is a 1 at the Hit output of the counter on every seventh clock pulse which is fed to the Switch Control block. The Switch Control block is a JK flip-flop in toggle mode. Hence the input of the switch is low for the first seven pulses and is high for the next seven pulses, and continues to be so.

When input to the switch remains high, PRBS output of length seven is obtained using tap t1 and when it is low another bit pattern is obtained using tap t2, which is also seven bit long. Hence the final output is a continuous PRBS of length sequence fourteen.

With a little addition of hardware circuitry the output sequence length could be extended to one hundred twelve, as shown in figure 3. The OR gates at the input of the flip-flops are used to feed the preset values.

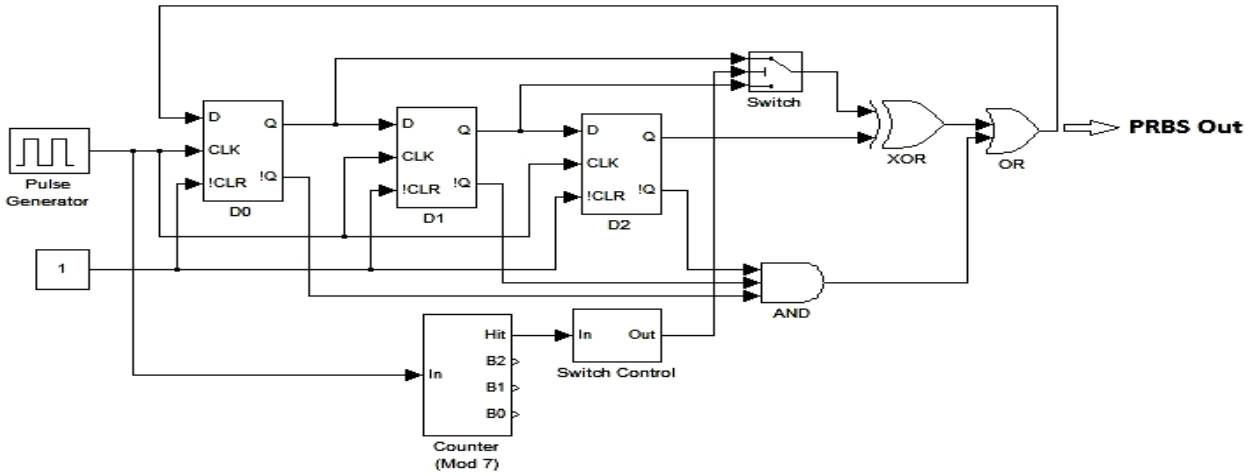

Figure 2: Block schematic of PRBS of length sequence 14

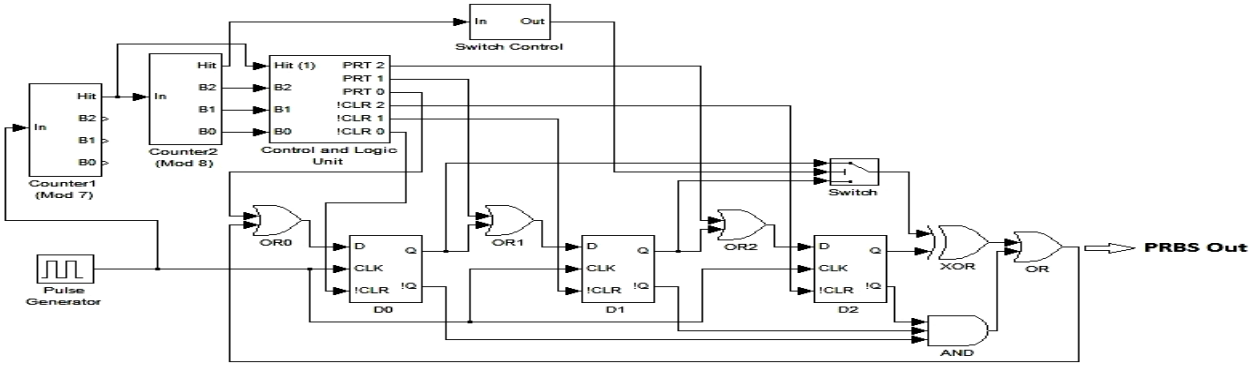

Figure 3: Block schematic of PRBS of length sequence 112

Detail of the Control and Logic Unit of the same is shown in figure 4.

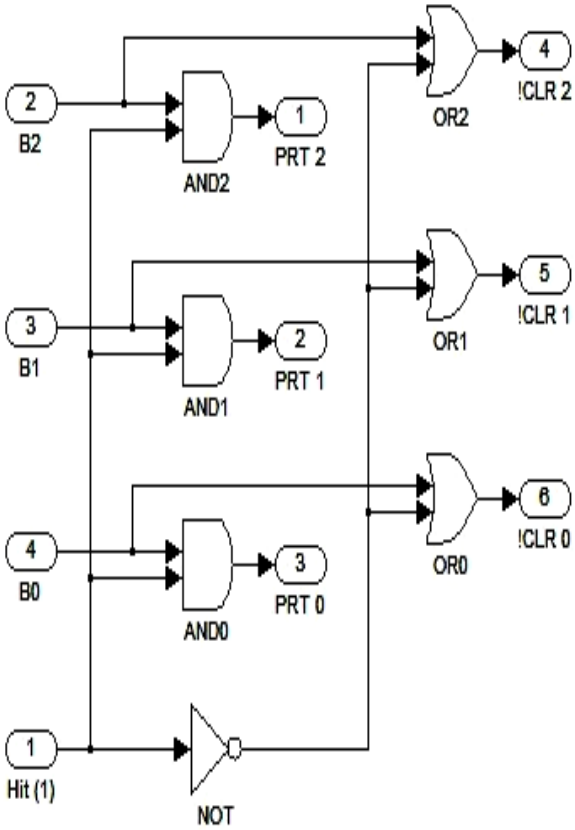

Figure 4: Detailed diagram of Control & Logic Unit

The explanation of the design is as follows. Here counter2 and the Control and Logic Unit are added to the previous counter stage. Whenever the Hit output of the first counter becomes high, the second counter increases by one. This second counter counts upto seven. Corresponding bits (B0, B1, and B2) are fed to the Control and Logic Unit. The outputs of this block are fed to the stages of the LFSR to originate particular preset values. These preset values change after completion of every maximal length sequence. The timing sequences of the preset and clear (inverted logic) signals with the used clock frequency are shown in **figure 5(a-g)**.

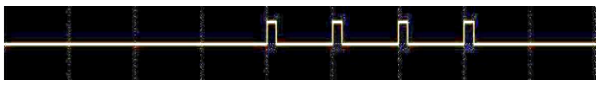

Figure 5a: PRT2

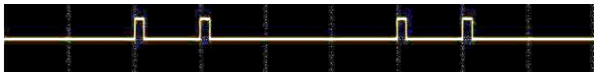

Figure 5b: PRT1

Figure 5c: PRT0

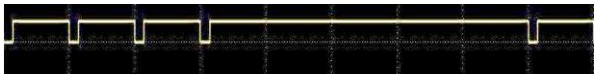

Figure 5d: !CLR2

Figure 5e: !CLR1

Figure 5f: !CLR0

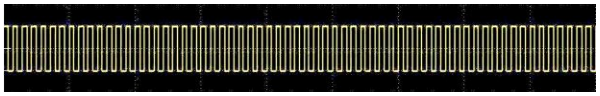

Figure 5g: Clock Frequency as Used

At the initialization of the circuit, the flip-flops are fed with a preset value of 000. After the first seven pulses, as the Hit value of the second counter increases by one the flip-flops are fed with the new preset values 001. This continues to increase upto 111. These values are repeated after every fifty six clock pulses. After the first fifty six pulses the output of the switch changes from zero to one. Hence the tap position changes after every fifty six pulses. Thus a PRBS of bit length one hundred twelve is achieved.

Corresponding time spans for seven bit, fourteen bits and one hundred twelve bits are shown in **figure 6**.

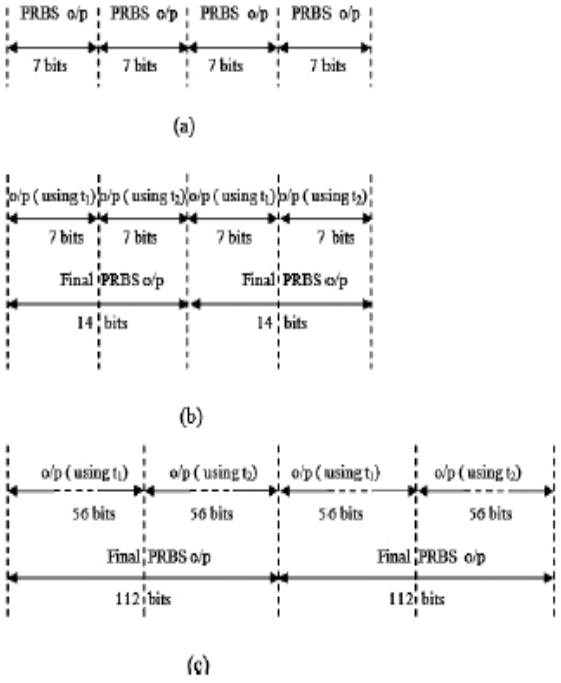

Figure 6: PRBS Timing Diagram for (a) figure 1 (simple LFSR: 3 stage) (b) figure 2 and (c) figure 3

4. Results

Figure 7(a-d) shows various simulation results in MATLAB SIMULINK. The PRBS outputs using different tap positions in a simple 3 stage LFSR are shown in figure 7a and figure 7b, using tap positions t_2 [3,2] and t_1 [3,1] respectively. The sequence length in each case is 7, though the sequences are distinct and different in nature. Figure 7c shows bit sequence of sequence length 14 and is obtained using figure 2. This sequence is a combination of the sequences of figure 7a and figure 7b respectively. The design, as shown in figure 3, generates a bit sequence of sequence length 112. The simulated output is shown in figure 7d.

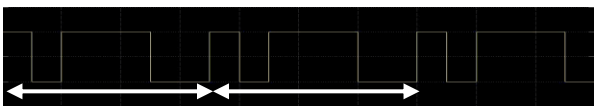

Figure 7a: PRBS of sequence length 7 using tap t_2

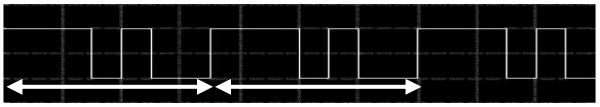

Figure 7b: PRBS of sequence length 7 using tap t_1

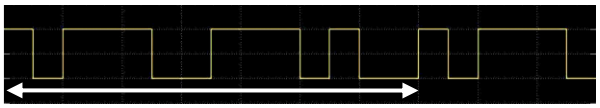

Figure 7c: PRBS of sequence length 14

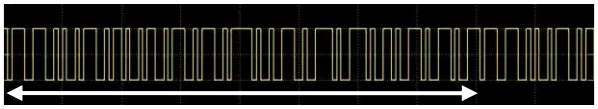

Figure 7d: PRBS of sequence length 112

5. Conclusion

The paper describes a 3 stage shift register configuration in feedback mode to generate multi maximal length sequences of different time periods. A simple three stage LFSR can generate a PRBS bit sequence of length seven only. Traditional LFSRs generate only one PRBS because the number of stages as also the tap position governs the output bit sequence. The present design allows one to extend this length to one hundred twelve. Also, there is provision for getting PRBS of lengths fifty six bits. Combining an up-down counter to the present design, the maximum length sequence can be extended to two hundred twenty four. A four stage LFSR can thus be effectively designed to get a PRBS output length of seven hundred twenty which can be extended to one thousand four hundred forty bits using an up-down counter.

The present design is not complicated, easy to implement and very economical in terms of hardware requirements. Again, the delays are much less in this case because only one intermediate tap is active at any given instant of time.

The PRBS generator will find extensive use in word synchronization, measurement of impulse response of a linear system by cross correlation technique, system identification, in encryption, spread spectrum radio and radar systems and also BER testing of I/O channels which require many PRBS strings of varied sequence lengths and periods. Thus a channel's effectiveness for data pattern dependencies and DC

imbalance can be more effectively evaluated because of considerable length of the generated PRBS output length sequence.

References

[1] A Chow, WS Coats, D Hopkins, "A Configurable Asynchronous Pseudorandom Bit Sequence Generator", 13th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 07), Page(s): 143 - 152, March 2007.

[2] S Kim, M Kapur, M Meghelli, A Rylyakov, Y Kwark, D Friedman, "45-Gb/s SiGe BiCMOS PRBS generator and PRBS checker [pseudorandom bit sequence] " Proceedings of the IEEE Custom Integrated Circuits Conference, Pages(s): 313 – 316, Sept. 2003.

[3] M Bussmann, U Langmann, WJ Hillerry, WW Brown, "A 12.5 Gb/s Si bipolar IC for PRBS generation and bit error detection up to 25 Gb/s" IEEE Journal of Solid-State Circuits, Volume: 28, Issue: 12, Page(s): 1303 -1309, Dec. 1993.

[4] H Knapp, M Wurzer, TF Meister, J Block, K Aufinger, "40 Gbit/s 2^7-1 PRBS generator IC in SiGe bipolar technology" Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, Page(s): 124 - 127, 2002.

[5] MG Chen, JK Nothoff, "A 3.3-V 21-Gb/s PRBS generator in AlGaAs/GaAs HBT technology", IEEE Journal of Solid-State Circuits, Volume: 35, Issue: 9, Page(s): 1266 - 1270, Sept. 2000.

[6] O Kromat, U Langmann, G Hanke, WJ Hillery, "A 10-Gb/s silicon bipolar IC for PRBS testing", IEEE Journal of Solid-State Circuits, Volume: 33, Issue: 1, Page(s): 76 - 85, Jan. 1998.

[7] WS Coats, R Drost, "Congestion and starvation detection in ripple FIFOs", Proceedings of Ninth International Symposium on Asynchronous Circuits and Systems, Page(s) 36 – 45, May 2003.

[8] SY Hwang, GY Park, DH Kim, KS Jhang, "Efficient Implementation of a Pseudorandom Sequence Generator for High-Speed Data Communications", ETRI Journal, Volume 32, Number 2, April 2010.

[9] MJ Miller, SV Ahamed, *"Digital Transmission Systems & Network, Vol. I: Principles"* Computer Science Press, 1987.

Aritra Sinha is presently a final year M Tech student in Instrumentation and Control Engineering from the Department of Applied Physics, University of Calcutta. He completed his B Tech from the same Department in 2011. He did B Sc with Honours in Physics from Dinabandhu Andrews College, Kolkata.

Sunit Kumar Sen is presently Professor of Instrumentation Engineering in the Department of Applied Physics, University of Calcutta. He graduated from St. Xaviers College, Kolkata in 1972 with Honours in Physics. Subsequently he did his B Tech and M Tech from the University of Calcutta in 1975 and 1977 respectively. He obtained his PhD (Tech) degree from the same University in 1993.

In 1978, he joined Bokaro Steel Plant (under SAIL) and served for more than five years as Assistant Manager, Instrumentation (Operation). In 1984, he joined the Department of Applied Physics as a Lecturer. His subjects of interest are Digital Electronics, Microprocessors, Digital Communication, Industrial Instrumentation, Electrical Networks, Fieldbus etc. He has around thirty four research papers in National and International journals. He has published two books: *Understanding 8085/8086 Microprocessors and Peripheral ICs Through Questions and Answers* and *Measurement Techniques in Industrial Instrumentation*, both published by New Age International (P) Limited, New Delhi. He is a life member of IETE, India.

He was Head, Department of Applied Physics and also USIC, University of Calcutta.