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Two-Port Transmission Line Parameters Approach Modeling and Design Centering of Integrated Continuous-Time Filters

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Abstract

Design centering is one of the important process followed for the accurate design of integrated continuous time filters where the filter frequency response is tuned to match the ideal in presence of non-idealities such as finite gain of the OTAs/Opamps and parasitics. One of the efficient method adopted is the space-mapping where the filter response is tuned in the 'model space' and the results are interpreted in the actual 'filter space' resulting in a time efficient process. This method demands the filter to be modeled and state-space approach has been the choice for modeling. This paper proposes a two- port transmission-line parameter based approach for modeling a class of filters. The paper compares the proposed process with that of the conventional state-space method. The demonstration is carried out on a 2nd order Butterworth low pass Gm-C filter having Cochlea architecture. The filter is designed to operate on a 0.5 V supply in 0.18 µm standard CMOS process. The paper brings out the limitations of state-space based approach for accurate modeling in the regime of low voltage design and demonstrates how the proposed two-port parameter based approach can be used for better accuracy.

Keywords

Design centering, Two-port transmission line, Continuous-time filters, State-space method, low-voltage

1. Introduction

According to Electronic Design Automation (EDA) magazine on March 21, 2005[1], analog components use, on average, 20% of the integrated circuit area and also reported that 75% of all integrated circuits would contain analog components. At the same time, the analog components require around 40% of the integrated circuits design effort and are responsible for about 50% of the design re-spins. Analog design automation is needed to improve the design quality and reduce the design effort, as more and more analog circuits are being integrated into ICs along with digital circuits. In view of these challenges there is need for a more efficient and reliable design approach to be followed in the field of analog circuit. These requirements drive the designers to rely heavily on CAD in order to reduce the time- to-design and errors in designing/modeling circuits. Like in any design cycle, the design of analog circuits (amplifiers, filters etc.) starts with a set of specifications. Architecture is then chosen to meet the specifications. The initial design of the circuit, typically, assumes ideal devices/elements. With this assumption a basic schematic is designed using CAD tools. However, the actual results from the schematic, when technology specific circuit elements are used, will deviate from the ideal. In CMOS circuits the deviation is normally attributed to finite $g_m r_0$ product of transistors and parasitic capacitors. It becomes necessary to design center the filter to achieve response that is in close match with the desired response even in presence of non-idealities. One such design-centering technique used for integrated continuous- time filters is presented in [2].

A simple design centering technique for integrated continuous time Transconductor-Capacitor (Gm − C) filters is presented in [2]. Due to the fully-differential architecture, chosen for this filter, the parasitic capacitance's appearing at the integrating nodes with-respect-to small signal ground have the dominating effect on the response. The effect of any inter-node parasitic capacitance is made small by design and a careful layout technique. The above assumptions make the design centering process simple which is evident from the paper. However, when the filter has a single ended architecture, for example Cochlea Architecture [3], the above assumption may not be valid if the inter node capacitance is a significant fraction of the integrating capacitor.

A course model is used for design centering the filter in [2] and is arrived using state-space approach. The state- space model of the filter is arrived by writing down the small-signal equivalent circuit. Transconductor is modeled as an equivalent circuit

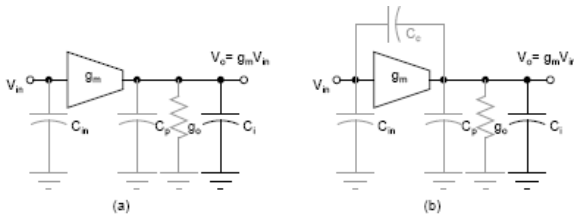

Figure 1: Equivalent circuit for non-ideal transconductor (a) Without gate-overlap capacitance (b) With gate-overlap capacitance

consisting of a tranconductance (g_m), output conductance g_0 , input parasitic capacitance C_{in} and output parasitic capacitance C_p as shown in Fig.1(a). It is to be noted that while modeling, the effect of overlap capacitances is neglected and is assumed that all parasitic capacitances appear in parallel with the integrating capacitors. If C_n is the capacitance value to be present at a given node for a desired frequency response, it is clear from the Fig.1(a) that the capacitance to be inserted (C_i) at that node can be easily found by subtracting total parasitic capacitance appearing at that node from Cn . In presence of gate overlap capacitance (C_c), the equivalent circuit of the transconductor can be drawn as in Fig.1 (b). In such a case the state-space model of the filter used in [2] will not be accurate enough due to following reasons- (a) possible frequency dependent Miller effect (b) addition of parasitic poles/zeros. It is not possible to adopt the design centering technique laid down in [2] as it is. In this paper an attempt is made to address this issue, especially in the regime of low voltage design. Scaling dimensions in CMOS technology require proportional scaling in supply voltage as well [4]. An important factor concerning analog circuit design is that the threshold voltage of transistors in future standard CMOS technologies does not scale with supply voltage and is projected to remain about 0.25 V [5]. With lower supply voltage, for example 0.5 V, there exist a voltage headroom issue due to higher threshold voltage and is found to be critical. In this situation the transistor may operate in weak inversion or in subthreshold region. In such a scenario while modelling circuits one need to consider subthreshold effects. Therefore the simple design centering technique proposed in[2] for filter operating at 3.3 V supply, that use state-space model is not suitable for circuits operating at low voltage if one needs to consider sub-threshold effects.

Two port parameter based representation is one of the methods used to model a linear system. This method can be readily adopted to model continuous-time filters as they are assumed to be linear for small-signal. Two-port transmission line parameter (ABCDparameter) model is one such method that can be effectively used for cascaded networks. This method is simple and has couple of advantages over other methods. Recent publications [6], [7] showed that there is increase in the application of two-port transmission line approach for better understanding of circuits.

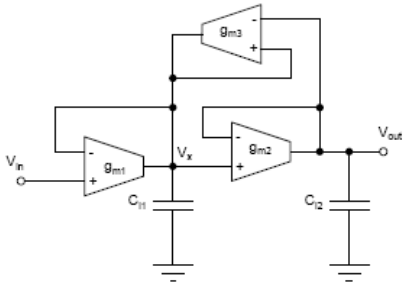

Figure 2: Schematic of Cochlea

In this work a bulk driven low voltage, low frequency Continuous- time Cochlea second order Butterworth low pass filter using Gm -C technique is designed. The filter is designed to operate at 0.5 V supply [8] and is used as a test-vehicle to explore the merits of two-port transmission parameter based modeling over state-space based approach for design centering the filter. The rest of paper is organized as follows. Section 2 details the architecture of Cochlea filter. Section 3 details the transconductor circuit design for the realization of 2nd order low pass filter. The state space approach and two port transmission line parameter used to build the model of the filter are given in section 4. In section 5 simulation results are discussed and conclusions are drawn in section 6.

2. Cochlea filter

The filter designed in this work use G_m −C approach and Cochlea architecture [3]. The schematic of second order low pass Cochlea filter is shown in Fig.2. g_{m1}, g_{m2} and g_{m3} are differential-in single-ended-out transconductors. C_{i1} and C_{i2} are the integrating capacitors. The transfer function V_{out} (s)

$$\frac{V_{out(s)}}{V_{in(s)}} = \frac{g_{m1}g_{m2}/C_1C_2}{s^2 + \left[\frac{g_{m1}C_1 + g_{m2}C_1 - g_{m3}C_2}{C_1C_2}\right]s + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad (1)$$

of the filter can be written as
The Cut-off frequency ω_0 and the Quality factor Q of the filter are

$$\omega_0 = \sqrt{\frac{gm1\, gm2}{C_1 C_2}} \quad (2)$$

$$Q = \sqrt{\frac{gm1\, gm2 (C_1/C_2)}{(gm1 - gm3) + gm2 (C_1/C_2)}} \quad (3)$$

It is clear from the expressions that the filter can be tuned for a given bandwidth ω_0 and quality factor Q by proper choice of transconductances and capacitance's. If the transconductors, realized, are bulk-driven, as is the case with this paper, the transconductances g_m in (1), (2) and (3) will be replaced by bulk-transconductances (g_{mb}).

3. Bulk-driven transconductor

The differential-in single-ended-out bulk-driven transcon- ductor used for the filter realization is shown in Fig.3.

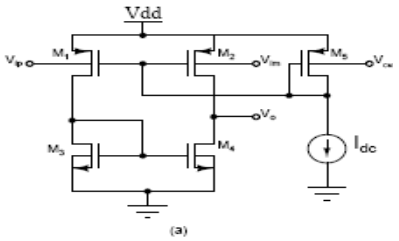

Figure 3: Schematic of Bulk driven Transconductor

M_1 and M_2 are the PMOS input transistors and M_3 and M_4 forms NMOS current mirror load. v_{ip} and v_{im} are the differential inputs and v_{out} as the single-ended output. The transconductor designed in 180 nm CMOS process to operate at a power supply of 0.5 V. The input common mode voltage of the transconductor is fixed at 0.25 V and the gates of M_1 and M_2 are biased to carry quiescent current of 2 µA. The designed transconductor provide a DC gain of 23.76 dB and has a Unity-Gain-Bandwidth (UGB) of 11.65 MHz.

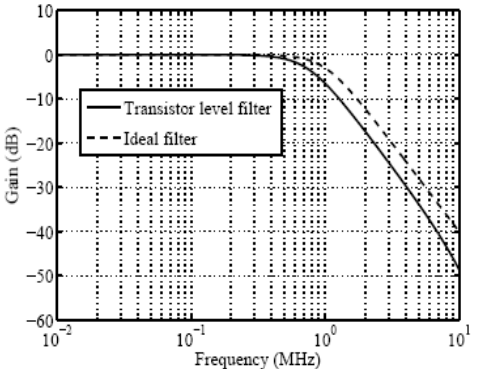

Figure 4: Magnitude response of Ideal filter and Transistor level filter before design centering

A Cochlea filter having Butterworth response is designed using above transconductor for a bandwidth of 1MHz. The integrating capacitors C_{i1} and C_{i2} decides the filter cut-off frequency under ideal conditions if transconductance is fixed as per (2) and (3). But non-idealities of the OTA like parasitic capacitance, finite output impedance and finite input impedance cause the frequency response to deviate from the Butterworth response. This effect is clearly seen in the magnitude response of filter shown in Fig. 4. Typically filter response is brought back to ideal or near ideal by tuning integrating capacitor with the help of design centering process. 'Space mapping' is one such technique that is proved to be effective for G_m-C filters [2]. This technique requires the entire filter to be modelled and as mentioned in the section 1, the state-space model is commonly used.

4. Model of the Cochlea filter

A. State-space approach based model

In order to analyze the limitations of the design centering process laid down in [2], the Cochlea filter is modeled in a manner similar to that given in [2]. The Equivalent circuit of the filter considering the finite output resistance is shown in Fig. 5. At the

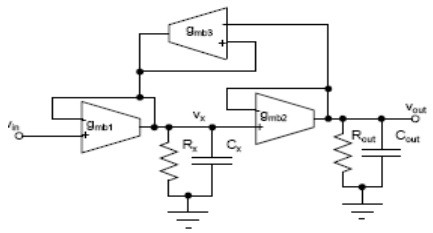

Figure 5: Equivalent circuit of the Cochlea filter considering the finite input and output impedance of the Trans conductor

intermediate node x, R_x is the effective resistance seen at node x and C_x is the effective capacitance seen at node x with respect to small signal ground which includes the total parasitic capacitances and intended integrating capacitor C_{i1}. Similarly at the output node, c_{out} includes parasitic capacitances and intended integrating capacitor C_{i2} . The state-space representation of the filter is given by (4) and (5).

$$\dot{x}(t) = Ax(t) + Bv_{in}(t) \quad (4)$$

$$y(t) = [0\ 1]\,x(t) \quad (5)$$

where, $x(t) = [v_x\ v_{out}]^T$ (6)

The state matrix A and the input matrix B of filter are written as follows.

$$A = \begin{bmatrix} -\frac{(gmb3 - gmb1 - 1/R_x)}{C_x} & \frac{gmb3}{C_x} \\ \frac{gmb3}{C_{out}} & \frac{(gmb2 + 1/R_{out})}{C_x} \end{bmatrix} \qquad R = \begin{bmatrix} \frac{gmb1}{C_x} \\ 0 \end{bmatrix}$$

The model is coded in Matlab. The resistance and transconductance values are taken from DC operating point analysis of the transconductor.

The filter is design centered using the approach proposed in [2]. First, the response is obtained for transistor level filter by simulating the filter with integrating capacitors C_{i1} and C_{i2} computed using (2) and (3). This response is then space- mapped to state-space model, where the model is tuned with C_{i1} and C_{i2} as variables to get a response that matches closely with that of ideal. The optimized values C_{i1} and C_{i2} are used in the transistor level filter. If the model is accurate, the the actual filter response will match with that of the model and ideal as well. In Fig.6 the response of the state-space model of the filter is compared with that of transistor level filter. The deviation in the response is an indication that the model is not accurate. This may be attributed to the additional parasitic poles and zeros formed by inter node capacitance in the transconductor and other secondary effects like sub-threshold effect. For better accuracy of modeling, the inter node capacitances and secondary effects have to be taken into account. For better accuracy every transconductor in the filer has to be modeled accurately. i.e. all the intermediate nodes and parasitics have to be taken into account. For the transconductor designed in this paper, it has an intermediate node formed at the common-drain point of M_1 and M_3 (refer Fig. 3). Therefore, considering the intermediate node, the small signal model of the transconductor can be written as in Fig.7.

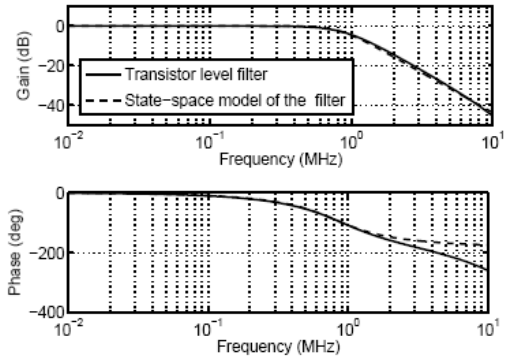

Figure 6: Frequency response of State space model and transistor level filter after design centering as proposed in [2]

The Cochlea filter used in this paper uses three transconductors and resulting in 6 state variables for the entire filter, while an ideal Cochlea filter has two integrating nodes (2 state variables). While modeling the filter, state-space matrices for the entire filter needs to be written carefully by selecting the state variable nodes. Analysis of such a complex circuit on paper is prone to error.

Two demerits are observed in modeling the filter using state space technique, with respect to small-signal model of the transconductor.

- Due to parasitic capacitances the actual order of the state space matrix will be more than that of the ideal situation (i.e without parasitics). As the order increases, writing state-space model will require too much of designers attention and time, which may lead to error in modeling.
- For low voltage supply, for example 0.5 V, the transistors in the Cochlea filter designed in this paper operate in sub-threshold region. Therefore in reality when modeled it is mandatory to consider sub-threshold effects for better accuracy. In state-space technique the filter is modeled using the small-signal equivalent circuit of the filter. It is necessary to model the transistors in the filter circuit by taking sub-threshold region of operation into account. If sub-threshold effects are need to be considered, for example secondary effects such as hot carrier effect, the model becomes more complicated.

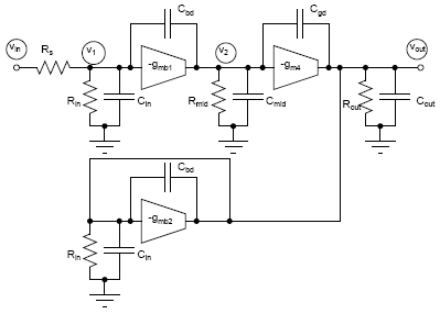

Figure 7: Small-signal equivalent circuit of the bulk-driven transconductor with parasitic nodes

For the Cochlea filter architecture considered in this paper and for similar architectures, there is need for a method to model the filter as accurate as possible at the same time keeping it simple for designers. A close look at the architecture of the filter reveals that, it can be considered as cascade of several two-port networks. It is well known fact that two-port transmission line (ABCD) parameter representation is the best suited two- port network model to represent cascaded two-port networks. It is worth exploring the usefulness of transmission line parameter modeling for the filter as an alternative to state- space model.

B. ABCD-parameter approach based model

A close look at the Cochlea filter shown in Fig.2 can be thought of as a cascade of four two-port networks as shown in Fig.8. The individual two-port networks are named as Sub block 1 - Sub block 4 in the figure. When ABCD-parameters are used to represent two-port networks, the ABCD model of the cascaded network can be easily obtained by simply multiplying ABCD matrices of individual blocks. i.e. if Ai, Bi, Ci and Di are the ABCD parameters of i^{th} Sub-block in Fig.8, the filter can be represented using ABCD-parameters as in (7).

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} \begin{bmatrix} A_4 & B_4 \\ C_4 & D_4 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (7)$$

The sub blocks 2 and 4 represent the capacitors and the ABCD-parameter

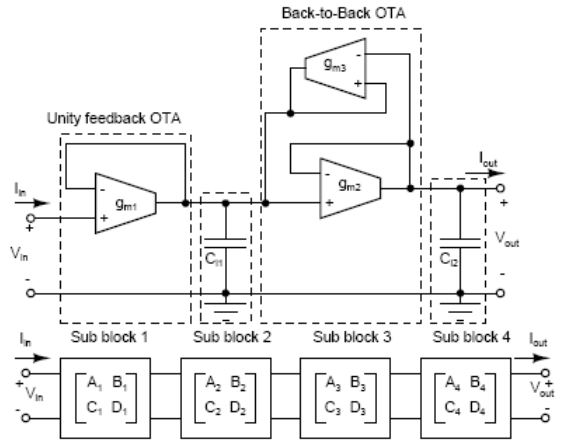

Figure 8: Cascaded two-port network representation of Cochlea filter

representation of these blocks is simple and directly available as given in (8)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ SC & 1 \end{bmatrix} \quad (8)$$

The matrix elements for the sub block 1 and sub block 3 are ratios of either voltage/current to current/voltage with port 2 open circuit or short circuit, small signal wise. With the help of cadence tool these ratios as function of 's' are found. This is intern done by finding the poles and zeros of A(s), B(s), C (s) and D(s) by appropriately open circuiting or short circuiting port 2 (small-signal wise). Once the poles and zeros are calculated one can discard the higher order poles and zeros whose effect falls out of frequency range of interest, thus reducing the computation complexity

Using above individual ABCD matrix elements, the ABCD matrix of entire filter is computed as below. The transfer function for the filter is $V_{out}(s)/V_{in}(s)$ for $I_{out}(s)=0$

This implies

$$\left[\frac{V_{out}(s)}{V_{in}(s)}\right] = \frac{1}{A_T} \quad (9)$$

Where

$$A_T = [A_1(s) + sC_{11}B_1(s)]A_2(s) + B_1(s)C_2(s) + [(A_1(s) + sC_{11}B_1(s))B_2(s) + B_1(s)D_2(s)]sC_{12} \quad (10)$$

Using Matlab the expression (10) of A_T can be evaluated. The computation of matrix elements C_1 and D_1 are not necessary as they are not part of A_T expression. We are interested in voltage gain of the filter, therefore the computations of the remaining matrix elements B_T, C_T and D_T are not required. As

compared to state-space method this method avoids the time spent with paper and pen in drawing and analyzing the small-signal equivalent circuit. It is found to be more accurate compared to the former method. With the use of CAD, the complexity involved in the modeling the filter with ABCD-

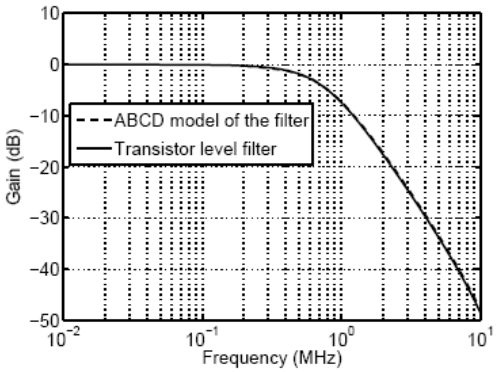

Figure 9: Magnitude response of ABCD model and Transistor level filter

parameter approach is found to be less, even with increase in the order of the filter. The frequency response obtained from the ABCD-parameter based model the filter and transistor level filter are shown in Fig.9. It can be inferred from Fig.9 that, the model response has one-to-one mapping with transistor level filter response for the entire range of frequency. Thus it is proved that the ABCD-parameter based model of the filter is accurate than the simple state-space model used in [2].

5. Results and discussions

Two models of the filter are obtained, one using state- space model approach and another using ABCD-parameter based approach and are used for design centering of the filter. Responses of the both models are obtained independently by tuning integrating capacitors C_{i1} and C_{i2}, to get response close to the ideal. So obtained optimized set of integrating capacitors are used in transistor level circuits. The response is plotted along with ideal response in Fig.10. From the inset in the Fig.10 it can be seen that the proposed two- port model based approach of design centering gives better accuracy than the state-space based approach. The small

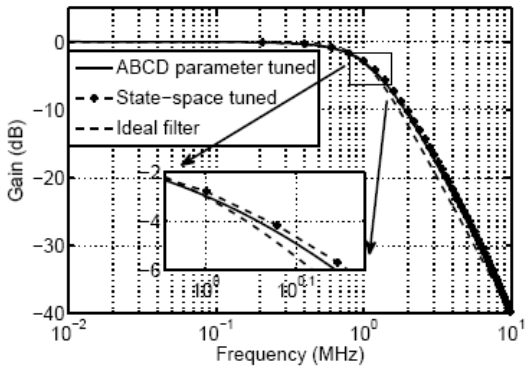

Figure 10: Magnitude response of Transistor level filter tuned with ABCD model, state-space and Ideal filter

deviation is due to the fact that the whole process of design centering attempts to match the response of a higher order filter (due to parasitics) to that of a second order filter. Fig.11 shows percentage error of the responses with respect to ideal. For the filter design centering using two-port parameter based approach the maximum error from ideal is found to be 22 % while for that obtained using state-space approach is 33 %.

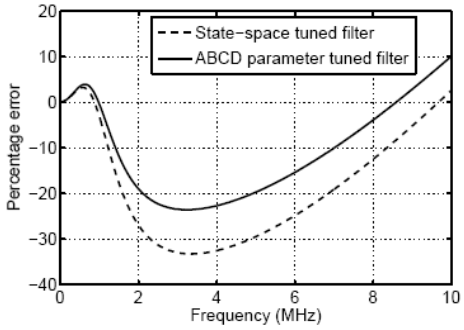

Figure 11: Percentage error with respect to ideal filter for Transistor level filter tuned with ABCD parameter model and state-space model

6. Conclusion

In this paper a two-port based modeming is proposed for design centering continuous time filter as an alternate to classical state-space model based approach. Both the proposed and classical method are used to design center 2nd order Butterworth low pass Cochlea filter designed in 180 nm technology for a bandwidth of 1 MHz to operate at 0.5 V. The outcome are compared and is found that two- port based approach using ABCD-parameter based model,

models the filter accurately compared to simple state-space based approach. It is also found that the proposed method gives better accuracy in terms of the matching of the filter response with ideal when compared to state-space model based approach. However the two-port based approach may not be applicable to all classes of filter especially where it is not possible to split the filter as cascade of two-port networks.

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