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Reconfiguration Challenges & Design Techniques in Software Defined Radio

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Abstract

The term 'Software Radio' was coined by Joseph Mitola III to signal the shift from HW design dominated radio systems to systems where the major part of the functionality is defined in software. It creates a necessity of generic programmable hardware base that would allow software to enable various features. The concept of Reconfigurable computing allows the acceleration of computational processes by using variable configurations of specialized hardware. The FPGAs are opening a new door in digital processing environments by providing Reconfigurability at different granularity levels. Further, the reconfiguration models reduce overheads present in traditional systems. Finally, the combination of both digital signal processing devices such as DSP/GPPs and FPGAs can take advantage of their respective features. These platforms provide ways to propose architectures for optimized SDR execution platform, which may reduce the SDR device size, power consumption and cost significantly while maintaining a high degree of design and function switching flexibility.

Keywords

Software Defined Radio (SDR), FPGA, Dynamic partial reconfiguration, Software Communication Architecture (SCA).

1. Introduction

Software Defined Radio (SDR) is the radio in which some or the entire physical layer functions are Software Defined [1]. The objective of developing SDR technology is to realize plural system standards on a single hardware platform that is implemented mainly with high speed programmable devices. In SDR the hardware module is reconfigured by the software module, which means that a given hardware platform is converted into specific system standard or special communication system depending upon the changes in the software module. [2

As wireless communication becomes more and more diverse, the need of software radio is getting stronger. The reason that wireless devices are so inflexible is that they are generally implemented is Hardware. Consequently, frequent redesign is expensive and inconvenient to the end users. So, the reconfigurable SDR can be obtained with either a single device capable of delivering various services or with a radio that can communicate with devices providing complementary services. [3].

2. Background & relevance

In the late 1950s Gerald Estrin came up with the concept of Reconfigurable computing which allows the acceleration of computational processes by using variable configurations of specialized hardware modules in addition to a sequential processing unit. Since 80's the Field Programmable Gate Array (FPGA) market growing rapidly with varied of application in different industries. The FPGA has great advantage of flexibility that comes from its programmable nature as compared to systems with application specific integrated circuits (ASICs).The prototyping of one or several applications can be done in different ways using a single FPGA as it incorporates memories, DSP in its architecture.

Reconfigurable computing is one of the techniques that fill the gap between hardware and software; it offers potentially much higher performance than software, with ability to maintain a higher level of flexibility than hardware [5]. This type of computing is based upon Field Programmable Gate Arrays (FPGAs). It contains an array of computational elements whose functionality is determined through multiple SRAM configuration bits. Like software, the mapped circuit is flexible and can be changed over the lifetime of the system or even the lifetime of the application. These elements, also known as logic blocks, are connected using a set of routing resources that are also programmable. [5].

3. Literature review

Reconfigurability challenges a number of areas ranging from users, business and regulatory aspects

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to radio resource/spectrum management and system level interactions. The technological challenges are not only on the enabling technologies necessary for the development of reconfigurable terminals and base stations but also on network and equipment architectures supporting Reconfiguration, reconfiguration management etc. [4]. Also, Reconfiguration through the software download over the air (OTA) is the most concerned issue to many researchers since its attractive concept of dynamic reconfiguration of SDR terminal can, not only be user friendly in subscribers point of view but also effective for network providers [3].
The case studies reviewed here, have proposed the different architectures in order to improve various parameters such as size of the software download OTA, memory overhead, reconfiguration time. The authors in [6] have proposed the architecture for GSM to EDGE reconfiguration using FPGA-DSP platform. The paper proves the feasibility of dynamic partial reconfiguration. The FPGA provides network switching by dynamically reconfiguring only from QPSK mapped Nyquist filter with to 8PSK mapped Nyquist filter.

The case study presented by authors [7] utilized TV white space which were made unlicensed in November 2008 by FCC. The paper concentrates on DFE (Digital Front End) module of SDR. The proposed SDR transmitter architecture is based on single FPGA and it is controlled by GPP. It uses DRP with PR on FPGA to support TV standards like 3GPP LTE, 3GPP WCDMA, IEEE 802.16.e; IEEE 802.11.n.While DRP with PR offers the functional reconfiguration along with programmable clock.

Along with reconfiguration, its management is one of the crucial factors. The authors in [8] proposed global architecture called Flexible Radio Kernel. The architecture has PL (Protocol Layer) and R-HAL (Radio-Hardware Abstraction Layer). Former manages the reconfiguration of MAC layer and later manages Platform reconfiguration.

The authors in [9] focused on the structure of reconfiguration facilitated by SCA standard. The paper includes simple AM/FM receiver that identify and receives either type of modulation. The modular applications of SCA are dynamically installed and uninstalled using CORBA middleware. This article addresses large-scale reconfiguration through Domain Management (facilitated by SCA), specifically, “waveform application management". In this level of reconfiguration, the waveform applications being run as SCA applications in the domain are dynamically installed and uninstalled based on the radio requirements. This approach reduces the hardware requirements of the radio (e.g. memory) but introduces latency.

4. Platform based design techniques

The design techniques involve hybrid platforms with different types of reconfigurations required as per application. The techniques highlight the advantages of dynamic as well as partial reconfiguration.

Using FPGA and DSP
DSP’s and FPGA’s provide the flexibility and the computational power required to realize a Digital Front End (DFE) of SDR [6]. FPGAs enable to take advantage of parallelism to achieve high performance with moderate power consumption. Furthermore FPGAs can be reconfigured in order to provide multi standard/service terminals.

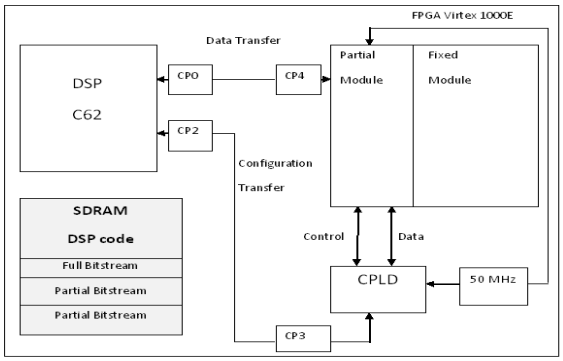

Figure 1: DSP/FPGA Sundance Platform

As shown in figure 1 the DSP and FPGA are connected through two Com- Ports, one dedicated to data transfers and the other dedicated to bit stream transfers i.e. for partial reconfiguration. In order to manage partial reconfiguration a CPLD is used to implement a configuration controller between the DSP and the FPGA.

In partial dynamic reconfiguration, only from a Nyquist filter with QPSK mapping to Nyquist filter with 8PSK is done. The hardware/software partitioning of the modulation chains (Figure 2) that have been considered for this study (QPSK to 8PSK) leads to the following decomposition. Software components, which correspond to source coding simulation, data transfers and configuration transfers, are mapped to the DSP. The hardware components, which are bits-to-symbol coding (mapping),

oversampling, filtering and IF transposition, are implemented in the FPGA.

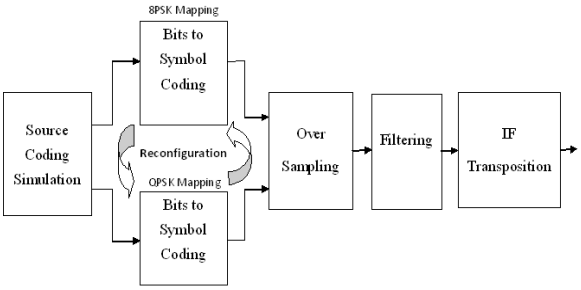

Figure 2: Partial dynamic reconfiguration on a DSP/FPGA platform

The bits-to-symbol coding component needs to undergo partial dynamic reconfiguration while other components are common to both modulation chains. The Virtex FPGA supports Colum based partial reconfiguration.

Table 1 presents the main characteristics of three scenarios. The first one does not implement reconfiguration; both chains are implemented in the FPGA. The second one uses dynamic reconfiguration but does not take benefit of partial reconfiguration (i.e., only full reconfiguration is performed). Finally, the last one uses dynamic with partial Reconfiguration. For each solution, the DSP memory overhead, the FPGA utilization and the reconfiguration time overhead are highlighted.

Table 1: QPSK/8PSK implementation scenarios

DSP/FPGA modulation chains implementation	**DSP memory overhead with bit stream**	**FPGA Utilization**	**Reconfiguration time overhead**
Without Reconfiguration	No	3180 Slices	No
With full Reconfiguration	1600 Kbytes	1590 Slices	130 ms
With Partial Reconfiguration	960 Kbytes	1590 Slices	11 ms

Between these solutions there is 50% reduction of the slice utilization. This is normal in our case since with reconfiguration a single chain is implemented at any time on the FPGA. The memory overhead in DSP occurring due to bit streams is an important issue for embedded systems. The use of partial reconfiguration leads to nearly 50% reduction in the DSP memory overhead. In the case of partial reconfiguration the DSP memory overhead is composed of one full bit stream and both partial bit streams (bits-to-symbol coding for the QPSK and the 8PSK modulations respectively) to be compared with two full bit streams in the case of full reconfiguration. Considering reconfiguration time overhead, partial reconfiguration leads to 90% reduction of the configuration time, which is very important in order to guarantee services continuity. Hence for an execution using dynamic partial reconfiguration of QPSK and then 8PSK modulations the benefit is almost 50% in terms of reconfiguration time. This benefit increases gradually when each time there is a new switching between both modulation chains.

Using FPGA and GPP

Partial Reconfiguration (PR) is a method for Field Programmable Gate Array (FPGA) designs which allows multiple applications to time-share a portion of an FPGA while the rest of the device continues to operate unaffected. The paper [7] presents a technique named Dynamic Reconfigurable Port (DRP), with PR based on a single FPGA in order to dynamically change both functionality and also the clock frequency.

Implemented Architecture

More recently new wireless opportunities such as TV White Spaces, opens a new area where SDR can be applied effectively.

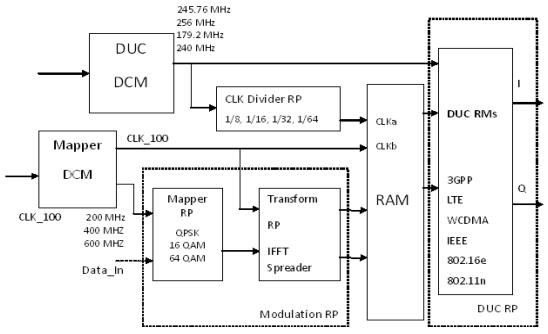

Figure 3: Implementation of SDR architecture to support three standards on FPGA

The secondary use of TV spectrum is unlikely to be driven by only one standard and therefore there exists the opportunity to support multi-standards at (low power) community base stations and use one FPGA hardware platform to potentially support multiple standards from TV White Space standards (IEEE 802.11-af, IEEE 802.22, 3GPP LTE-TDD).

Example architecture shown in figure 3 has been developed to support 3GPP LTE, 3GPP WCDMA, IEEE 802.16e and IEEE 802.11n standards. Two DCMs with DRP are employed: one is used to control and configure the mapper RP, and the other is for the DUC RP. The mapper DCM uses the input clock of a 100 MHz crystal oscillator for the generation of three clock frequencies: 200 MHz for QPSK, 400 MHz for 16-QAM and 600 MHz to serve 64-QAM modules. The data output by the mapper RP can then be fed to the transform RP operating at a clock frequency of 100 MHz for the WCDMA implementation, the spreader modules contain the OVSF code generator with SFs from 4 to 512.
Two simple dual port Block RAMs are used to bridge the clock domain boundary between the modulation processing components and the DUC RP. The 256 MHz from the clock oscillator is chosen as the input clock for the DUC DCM component so that by setting different integer multiplier and divisor values, the output frequencies of 245.76 MHz, 179.2 MHz and 240 MHz may be derived from this frequency correctly.

Table 2: Hardware utilization in terms of Slices

Mapper	Standards	Utilization without PR (Slices)	Utilization with PR (Slices)
QPSK, 16QAM, 64QAM	3GPP LTE 5 MHz	799	637
QPSK	3GPPWCDMA	722	566
QPSK, 16QAM, 64QAM	IEEE 802.16e 3.5 MHz	869	648
QPSK, 16QAM, 64QAM	IEEE 802.16e 5 MHz	817	634
QPSK, 16QAM, 64QAM	IEEE 802.11n 20 MHz	555	490
Modulation	OFDM	797	748
	Spreader	13	15

In the paper all of the designs are implemented on the Virtex -5 series LX110T device with Xilinx ISE 12.4 software suite version. Table 2 gives the hardware resources utilization of each of the modules without and with PR in terms of slices. There is approximately 20% reduction in slice utilization using PR. As a result, this PR/DRP architecture could be viewed as providing a high degree of function switching and design flexibility. It uses fewer clock oscillator inputs are required compared to traditional, fixed function FPGA design. Therefore, the proposed method could reduce the SDR device size, power consumption and cost significantly, while maintaining a high degree of design and function switching flexibility

Using flexible radio kernel
The aim of a flexible radio device is to offer reconfigurable radio operation flexible radio is a very wide concept. it encompasses any solution for radio operation that can be modified without changing the physical system. [8]

Proposed Global architecture: Figure 4 shows global FRK architecture. The Protocol Layer (PL) acts as a networking standard scheduler in FRK. . It stores all implemented MAC layers, and controls activation or inactivation of each MAC layers. The Radio Hardware Abstraction Layer (R-HAL) acts as an inter-face between the operation implementation and the upper layers, managing the reconfiguration and the control of the physical layer resources allocation. FRK is based on the definition of targets in the platform. A target is a type of processing units for which the configuration method is similar. Each platform is made of a collection of targets, for which the R-HAL implements a Target Management Element (TaME), designed to manage configuration and execution on the target.

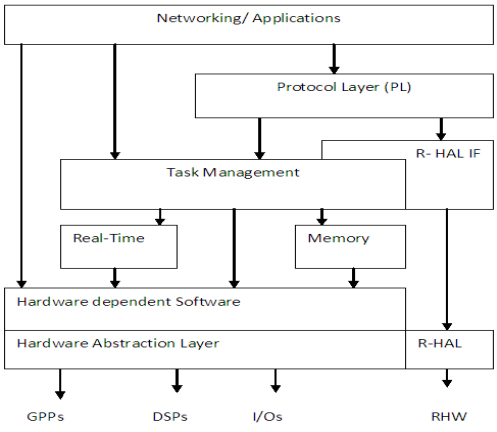

Figure 4: FRK global architecture

The off-line part is integrated in the R-HAL. It is designed to translate a generic application called a waveform into a platform executable called a Configuration Instance (CI). The R-HAL is designed to manage reconfigurability in a flexible radio

platform. It offers to the PL and other possible layers an abstracted interface for application management. It manages the instantiation of multiple applications and the repartition on the different targets according to the platform capabilities. The aim of R-HAL is to manage the configuration of the platform following requests from the PL. Thus, the environment allows easy integration of heterogeneous processing units.

Using SCA Architecture

The software defined radio (SDR) has opened the doors for levels of radio reconfiguration not possible through the use of more traditional radio design approaches. While most radios allow variation of parameters such as carrier frequency, an SDR enables large-scale reconfiguration (e.g., changing to a different protocol type or MAC). This research explores automated, dynamic large-scale radio reconfiguration through the implementation and characterization of three alternative reconfigurable radio designs.

The SCA is a widely used SDR standard developed by the US Department of Defense. The paper [9] includes simple AM/FM receiver that identify and receives either type of modulation. The modular applications of SCA are dynamically installed and uninstalled using CORBA middleware. Two methods for system reconfiguration are considered. In the first method, the installation of SCA applications is variable during runtime. A hybrid method combining these approaches can be considered, in which the radio anticipates the most immediately useful subset of available SCA applications.

Design Approach: Reference design accepts a baseband signal that can be either FM or AM using large scale reconfiguration. These receivers are capable of determining the modulation type of the signal and demodulating the signal appropriately.

Case 1: Modular multi-mode receiver with dynamic Reconfiguration (steady state):
As shown in Figure 5, specifically the signal classifier component is able to install/uninstall as well as connect to/disconnect from the AM and FM receiver components during runtime. With these abilities, the signal classifier is able to manage the state of the AM and FM receiver applications so that only the required receiver is installed at any given time.

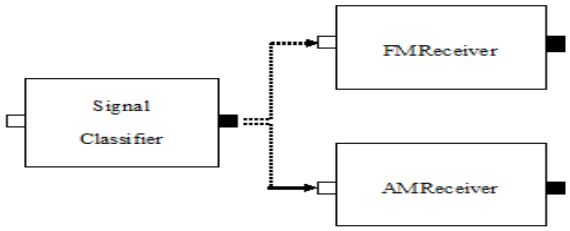

Figure 5: Modular multi-mode receiver

In this method, whenever the configuration of the radio changes, any existing SCA application that is no longer needed can be uninstalled and disconnected, and a new SCA application installed in its place. Using this method, only SCA applications that are actively processing data are installed. This approach exhibits minimal Memory usage when only one SCA application is installed at a time. The worst-case latency performance occurs for the extreme case in which the required SCA application must be installed and uninstalled every time a packet is sent or received.

Case 2: Modular multi-mode receiver with dynamic Reconfiguration (during reconfiguration):
Applications considered likely to be used are kept installed until supplanted by other applications as measured using a likelihood-of-use metric. In this extended dynamic approach, waveforms are installed and uninstalled less frequently provided that more than one waveform can be installed at a time and data are routed to the appropriate installed waveform. In this design, only one receiver SCA application is installed at any given time. When the radio switches operating modes, the existing receiver SCA application is uninstalled and the new receiver SCA application is installed in its place. Signal classification is accomplished by calculating the variance of the magnitude of the baseband signal. Since the FM signal theoretically has a constant envelope in the absence of noise and fading, if the variance is low, the signal is determined to be FM. Alternatively, the signal is determined to be AM.

5. Discussion

As per discussed case studies, we can summaries that different platforms use different reconfiguration techniques enlisted in Table III. The platforms provide reconfiguration of modulation chain, application switching, and multi service and reconfiguration management.

Table 3: Discussed Parameters

Sr. No.	Published Year	Platform Used	Application	Reconfiguration Used
1	2004	FPGA and DSP	QPSK to 8PSK	Dynamic partial reconfiguration
2	2010	SCA	AM/FM switching	Dynamic reconfiguration
3	2011	FPGA and GPP	3GPP LTE, IEEE802.16e, ,3GPP WCDMA, IEEE802.11n	DRP with Partial reconfiguration
4	2012	FRK	Reconfiguration Management	Level Dependent

6. Conclusions and Future Work

As per the discussion, the platform comprising of FPGA and DSP offer two advantages. As DSP works as hardware accelerator for FPGA, increases the speed of reconfigurable functionality. Also, FPGA due its partial reconfiguration ability reduces size of software to be downloaded locally or over the Air (OTA) which in turn contributes to solve the challenge mentioned in[2]. In platform consist of FPGA and GPP, the FPGA supports the multiple TV white space standards. As the standards require different frequencies to operate, the authors presented an architecture which uses DRP with PR to reconfigure clock along with functionality. The GPP handles the user requirement and decides which partition is to be reconfigured. The Flexible Radio Kernel provides an environment for easy reconfiguration management. This platform can be employed where there is necessity for management of reconfiguration. The SCA architecture facilitates different modular application to build on single platform and to run it independently. The case study discusses an receiver architecture that receives either AM or FM depending on variance using dynamic reconfiguration.Thus, Dynamic and Partial reconfiguration is an interesting solution to conquer the challenges in SDR reconfiguration.

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