International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970)
Volume-3 Number-3 Issue-11 September-2013

Field Programmable Gate Array based Simultaneous Temperature-Visualization on Video Graphics Array Monitor for Multi-Sensor Data Acquisition System

P.K. Gaikwad

Abstract

The present paper depicts visualization of temperatures on Video Graphics Array (VGA) monitor; using no central processing units (CPUs). It displays the temperatures sensed by multiple sensors, concurrently. Instead of reading the physical parameters on numerical display panels, or observing those on a personnel computer (PC) based system; the instrumentation was developed in such a way that, temperatures were displayed in the form of bar graphs on VGA monitor. The number of such strips indicates various data acquisition systems built around a single Field Programmable Gate Array (FPGA) chip. Different Soft Intellectual Property (IP) Cores were implemented in the Xilinx FPGA, Spartan 3E device, to drive 12 bit serial Analogue to Digital Converters (ADCs) and a VGA monitor; having 480 by 640 pixels resolution. Two AD7991 boards were interfaced with the FPGA chip; providing necessary signals for the Inter IC (I2C) serial communication protocol. Each degree centigrade (°C) of the temperature was scaled to 4 pixels on vertical axis, meaning thereby, a 30°C was represented by 120 (30x4) pixels; illuminating vertically on the VGA monitor. A growth of one °C increases row address by the figure of 4, maintaining the column address on VGA monitor.

Keywords

ADC-AD7991, FPGA, concurrent, temperature, VGA monitor

1. Introduction

The physical parameter like temperature is often essential to visualize immediately to the observer. The heating systems may be observed on a common display unit. In case, a trained supervisor is unavailable, it is critical to read display panels and take necessary action; if any heating system attains the precarious temperature.

P.K. Gaikwad, Department of Electronics, Willingdon College, Sangli, Affiliated to Shivaji University Kolhapur, (Maharashtra) India.

Instead of observing the numerical values of temperature, it is very easy for a trained, untrained supervisor, or even any illiterate viewer if it is made to have a look at color strips; changing their heights on a Video Graphics Array (VGA) monitor according to the temperatures of various heating systems.

To perform data acquisition on electric signals relating to temperature, a set of temperature-sensors is required. When the processing-system is designed by a microcontroller or a Personal Computer (PC), the sensors output are processed in a sequential manner. The output of data acquisition system has to be produced on a display unit for visualization purpose. It may be accomplished using either a numerical display panel; assembled using several seven-segment displays, or a multi-channel oscilloscope; showing temperature variations in the form of a constant or undulating line. It may be also possible that, various bar-graphs on LED strips indicate the level of temperatures. A classy display panel of VGA monitor may be obtained deploying a PC; installed with a data acquisition setup with necessary hardware and software.

In either of the multi-sensors driving system with any of the display types mentioned so far, it requires a dedicated display unit. Also using the Personal-Computer (PC) based system; it engages the entire PC and display unit for continuous monitoring the temperatures. The bottleneck is that, only one data acquisition system can work at a time. This occurs due to the sequential nature of the systems; constructed either using a microcontroller unit or a PC based instrumentation. The system described in [1] provides four voltage channels at 12-bit resolution, and operates over the temperature range experienced by a radiosonde from the surface to lower stratosphere. The analogue-to-digital conversion is supervised by a programmed microcontroller, which also formats the data for serial transmission through a modem. On the other hand, a research group [2], describes a Laboratory Virtual Instrument Engineering Workbench (LabVIEW) based data acquisition and analysis developed specifically for radial temperature distribution. Even though the temperatures were simultaneously

measured and displayed; the deployment of entire PC system is mandatory.

The present research work focuses performing simultaneous data acquisition process over multiple temperature sensors. The real-time variations of sensor-signals were visualized on a VGA monitor; without any Central Processing Unit (CPU) being used in Personal Computers. The concurrent nature of Hardware Description Language (HDL) executing more than one processes, architectures, or entities instantiated in a top level module, has played a vital role in this research. The electrical signal-variations of sensors were shown in the form of bar-graphs on a VGA monitor; whose tallness varies according to its related temperature. Two serial Analogue to Digital Converter (ADCs) chips AD7991 were driven by Soft Intellectual Property (IP) Cores, as given in [3]. A process of generating horizontal and vertical synch pulses; required to perform Raster scanning on the VGA monitor, was executed by another Soft IP core provided in [4]. The essential binary signals for red, green and blue colors were supplied to enlighten appropriately addressed picture cells (pixels) on VGA monitor. For that, a Very High Speed Integrated Circuit HDL (VHDL) entity was developed as a major role of this research.

The 12 bit serial data, emerging from the ADC chips; pertaining to the amplitudes of analogue signals of temperature sensors were input to the Field Programmable Gate Array (FPGA) chip. A top level entity was designed by instantiating different Soft IP Cores. One of the integrated modules drives the serial ADC chip and converts the 12-bit serial data into its parallel form. The magnitude of this 12 bit data varies the height of corresponding strip shown on the VGA monitor; driven by another VHDL entity, providing necessary signals to drive the VGA monitor. As there are two temperature-sensors, two vertical strips were shown on the screen; changing their heights with respect to the temperatures. The present research proves that, it is possible for number of heating systems to display on a PC-less VGA monitor; that too performing data acquisition process concurrently. Thereby, it reduces the chances of missing any hazardous upsurge in the temperature of any of the heating system.

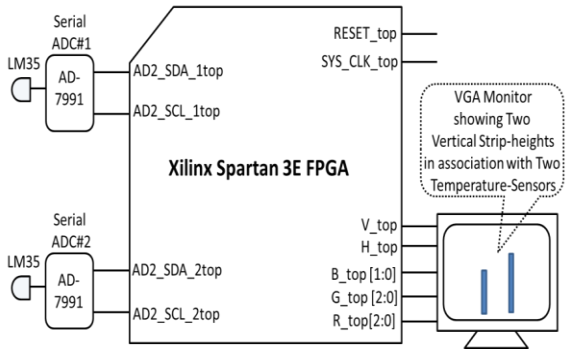

Figure 1: FPGA based temperature indication on VGA monitor for multi-temperature sensors

2. System Overview

The vital organ of this research is not just to visualize or indication of some physical parameter on a display unit; but to perform simultaneous data acquisition process as well as display its outcome on a PC-less VGA monitor. On the other hand, an embedded box containing ADC and FPGA setup does not make it essential to carry the dedicated display unit with. Any VGA monitor having pixel resolution of 480x640 can be plugged with such system and observe the change in temperature; sensed by multiple sensors, in the form of vertical strips. The Fig. 1 illustrates two LM35 temperature sensors, each connected with a 12 bit ADC chip AD7991. The serial information emerging from each of the ADC output lines i.e. *AD2_SDA_1top* and *AD2_SDA_2top* was given as input to the Xilinx FPGA device, Spartan-3E. Both ADCs were driven by individual Soft IP Cores; integrated together in the FPGA and provide necessary ADC-driving signals on *AD2_SCL_1top* and *AD2_SCL_2top*.

As given in [7], the Nexys2 board uses 10 FPGA signals to create a VGA port with 8-bit color and the two standard sync signals (HS–Horizontal Sync, and VS–Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create eight signal levels on the red and green VGA signals, and four on blue (the human eye is less sensitive to blue levels). To provide red, green and blue signals, there were lines connected to the VGA monitor adapter (DB 15 connector) from FPGA pins; configured as output. To perform the horizontal and vertical scanning of electron beam as explained in [5], the necessary signals named as *H_top* and *V_top*, were provided to the VGA monitor from the FPGA. Fig. 1 shows two vertical lines on VGA monitor with

different heights. It reveals the output voltage-magnitudes of two temperature sensors. A system clock (named as *SYS_CLK_top*) of 50 MHz; available on the FPGA board was provided to the top level VHDL module, which was implemented in the Xilinx FPGA device Spartan 3E.

3. Integration and Development of Soft IP Cores for the Top Level VHDL Module

A soft IP core given in [3] was instantiated in the top level VHDL module to perform the analogue to digital conversion using ADC chip AD7991; requiring Inter IC Communication (I2C) protocol signals. A 12 bit serial data, associated with the magnitude of analogue input voltage was generated at its output line. It was serially collected in the FPGA and stored in an internal buffer. A set of two temperature sensors LM35 was connected at input of two different ADC chips; driven simultaneously by FPGA.

As there is a 12 bit ADC, its step size was calculated by dividing its reference voltage (3.3V) by 2^{12} (4096), which results to 0.805 mV. The temperature sensor IC-LM35 generates voltage of the order of 10 mV per degree centigrade [6]. Therefore, decimal equivalent of 12 bit binary value for one degree centigrade (°C) was calculated by dividing the sensor output voltage 10 mV (per °C) by the step size of ADC, and it results approximately 12.5. On the other hand, to obtain the decimal equivalent for a given temperature, this 12.5 number was multiplied with the temperature value. For example, at 25 °C, the decimal equivalent of a 12 bit binary number becomes 12.5x25= $(312.5)_{10}$. However, in present research work for development of soft IP core, this 312.5 figure was rounded as 312. That means, greater than this number would indicate the temperature of 26 °C or above. A VHDL code line given below indicates that, for presenting 25°C temperature, the decimal equivalent of 12 bit binary data (obtained from internal buffer of ADC-driving module) should be in the range of 301 to 312.

TEMPinDegree <=25 when (ADC_out_sig > 300 and ADC_out_sig < 313) else -- 301 to 312 (25 deg)

It shows that, an internal signal *TEMPinDegree* is assigned an integer value 25; for satisfying the given condition. This condition is shown on right hand side (RHS) of the signal assignment operator (<=). Such a signal was passed onto another process named as RGB; that decides the height of visualizing-strip on the VGA monitor. Each degree centigrade of temperature was vertically scaled to 4 pixels on the screen.

The maximum row address (480) is at the bottom of VGA monitor (used in this research), and maximum column address (640) is at its right side. The following part of the VHDL entity named as *parameter_VGA* shows two distinct 'case' statements used in VHDL process: *RGB*. It elucidates that, when integer value 1 is assigned to the internal signal *TEMPinDegree* in the combinational part of the architecture (Behavioral), then pixels of row address in the range of 457 to 459, and column address 301 to 319 were selected to enlighten. These addressed pixels were made green by providing a 3 bit value "111" to the signal named as *green*. On the other hand, when the signal *TEMPinDegree* accumulates the integer 25, pixels of the row address range 361 to 459, and the same column address i.e. between 301 and 319 were made green to elevate the strip-height, vertically.

```
RGB: process (row, column, TEMPinDegree)
begin
case TEMPinDegree is
when 1 => if (row > 456 and row < 460 and
            column>300 and column < 320)  then

                red <= "000";
                green <="111";
                blue <="00";
          else
                red <= "000";
                green <= "000";
                blue <= "00";
          end if;
…
when 25 => if (row > 360 and row < 460 and
              column > 300  and column < 320)
        then
                red <= "000";
                green <="111";
                blue <="00";
           else
                red <= "000";
                green <= "000";
                blue <= "00";
           end if;
```

The accumulations of odd integers in signal *TEMPinDegree* were illustrated with green color strips, whereas for even numbered cases, red and green signals both were provided 3 bits of "111". Such strip-color variations on the VGA monitor for each successive integer value was to realize the

change in the temperature by each degree centigrade and visualize it easily.

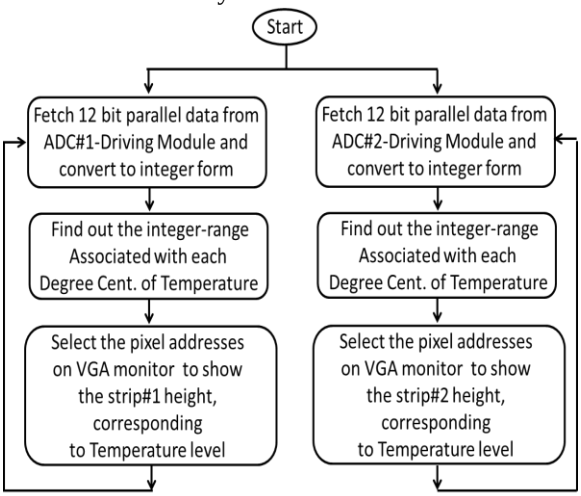

Figure 2: Development and Implementation Flow of Soft IP Cores for indication of two temperature sensor-signals on two strips on VGA monitor

Each set of the 4 pixels enlightening vertically pertain to 1°C temperature. The difference between lowest row addresses in case of signal *TEMPinDegree* having value 1and 25 is 457-361= 96. Addition of number 4 of the first case (*TEMPinDegree*=1) produces value 100. Dividing the number 100 by 4 pixels, that is, the difference between pixel addresses used for subsequent cases of each degree centigrade, it results 25. That is, to display temperature of 35°C it takes 35x4= 140 pixels vertically. There is no change in address range of columns; it remains 301 to 319 for one temperature sensor. For another module of data acquisition system, the column address was added with a figure of 100 i.e. the range was 401 to 419.

The Fig.2 shows two data acquisition systems working simultaneously to display two strips on VGA monitor. It shows that for one strip display, initially it fetches a 12 bit parallel data from ADC driving module number 1, and converts to integer form. A predefined range of such an integer, for example, 301 to 312 was used to represent 25°C temperature. This was reflected on the height of a strip displayed on part the VGA screen. Another module as shown in Fig.2 performs the same operations, but it senses the temperature from another sensor and reflects the parameter on another vertical strip on the same VGA monitor. This concurrent nature of executing number of entities is one of the real-potentials behind the Hardware Description Languages, HDLs.

4. Synthesis Results of the Top Level VHDL Module

The Fig. 3 illustrates Register Transfer Level (RTL) Synthesis result; screening four different VHDL modules instantiated together to develop a top level entity, named as *parameter_VGA*. It comprises two entities *VGA2_strip*, *VGA1_strip*, whose instance names are *VGA_Disp2* and *VGA_Disp1*, respectively. They provide necessary pixel addresses and enlighten them in the form of vertical strips; varying their heights according to the magnitudes of 12 bit signals. This signal was obtained from serial ADC-AD7991 driving-modules, named as *master1Controler* and *master2Controler*. Serial ADC chips were driven by FPGA using Inter IC (I2C) serial communication protocol. The VGA driving modules provide 3-bit *red*, *green* beam signals; however, the 2 bit signal was given for *blue* colour beam to illumine the selected pixel on the VGA monitor with proper colour. As shown in Fig.3, the outputs of VGA driving entities are logically *OR*ed together, and final signals from FPGA pins: *B_top(1:0)*, *G_top(2:0)*, *R_top(2:0)*, *V_top* and *H_top* were obtained. The interconnection between Xilinx FPGA Nexys2board and VGA pins are explained well in [7].

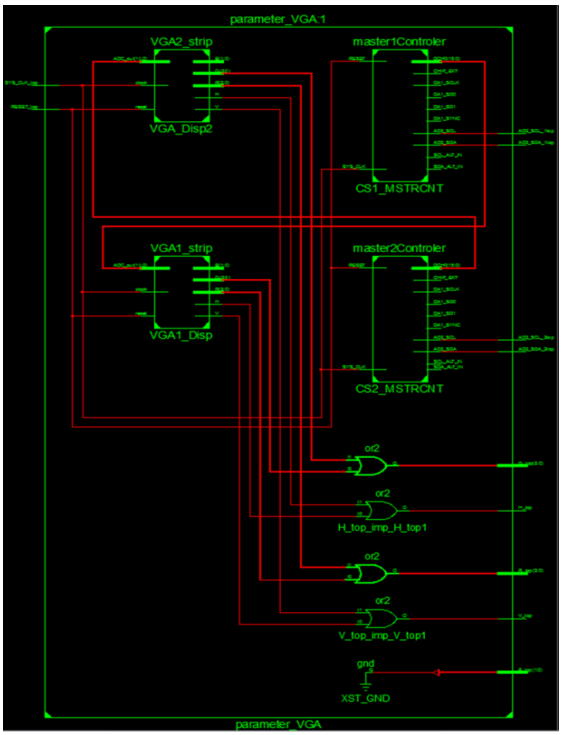

Figure 3: A Synthesis Result at Register Transfer Level (RTL) showing Integrating Soft IP cores.

5. Final Testing of the System

The Fig. 4 illustrates a complete hardware setup to monitor temperatures sensed by two LM35 devices. One of the temperature sensors was placed in touch with a heating soldering iron, and another LM35 was kept free to air and sense the room temperature. The analogue outputs from both of the sensors were connected to individual digital multimeter (DMM); set to measure voltage in the range of 0 to 2 Volts. The analogue channel number 0 of distinct ADC modules were also connected at the output of these sensors. The Xilinx FPGA Spartan 3E board: Nexys2 provided from Digilent Inc. was interfaced with AD7991 modules and VGA monitor.

As given in [6], when the voltage shown by LM35 output-pin (in millivolts) is divided by 10, it gives the temperature value in degree centigrade. Consequently, as shown in Fig. 4, the DMM reading V_{A1}=0.284 V (284 mV) can be treated as temperature of the order of 28.4°C. Similarly, by using another DMM; displaying analogue voltage (V_{A2}) of the order of 795 mV was used to find temperature value 79.5°C. Further, such different temperatures were rounded in integers. That is, 28.4°C was taken as 28°C, and 79.5°C was treated as 80°C. This arrangement was to provide the information (about analogue voltages belonging to the temperatures) to the soft IP cores implemented in the FPGA. The VGA monitor as shown in Fig.4 displays distinct vertical strips with dissimilar heights in accordance with the temperature values sensed by two LM35 devices. The pixels row address range for visualization of 80°C was 145 to 459, i.e. total addressed pixels (vertically) were 316. A group of 4 pixels represent 1°C temperature here. Thus, dividing the figure 316 by 4 results 80; which is the temperature sensed by device LM35; kept in contact with heating iron. The VHDL module, changing height of the strip as per the 12 bit data it receives was coded in such a way to make the colour strip red; as soon as the temperature exceeds the pre-set value of 59°C. Therefore, the red colour strip was seen on the VGA monitor for 80°C (greater than 59°C). On the other, a green strip having the height of just 112 pixels on the same screen indicate 28°C. Each of the strips was having 100 pixels to display pixels horizontally.

6. Conclusion and Future Work

The present paper deals with development of an FPGA based system that deals with two temperature-sensors and represent such parameters on a CPU-less VGA monitor. This helps inspecting the given parameter in a different and easily monitoring form than the existing systems. Such a prototype can be also useful for humidity monitoring and many other physical parameters on the same VGA monitor; concurrently.

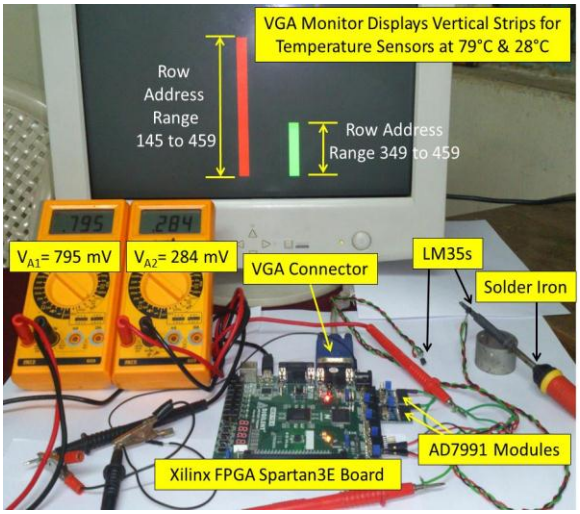

Figure 4: A complete hardware setup to exhibit distinct temperatures simultaneously on the VGA monitor

Acknowledgment

The present paper shows the potential of Hardware Description Languages (HDLs) executing more than one entities or processes in it; concurrently, which is not possible in sequential systems like microcontroller, or PC driven systems. The prototype developed here depicts.

References

[1] R. G. Harrison, "Inexpensive multichannel digital data acquisition system for a meteorological radiosonde", REVIEW OF SCIENTIFIC INSTRUMENTS 76, 026103 (2005), American Institute of Physics. [DOI: 10.1063/1.1841971].

[2] Ahmed Mudher Hassan , Hazem I. Ali & Ali Farooq Lutfi, "A Lab VIEW Based Data Acquisition System for Radial Temperature Distribution", IJCCCE, VOL.9, NO.1, 2009.

[3] Support Document, "Xilinx ISE demo project for the PmodAD2 and a PmodDA1", Digilent Inc., Pullman, WA 99163-0428, November 2011, DSD-0000321.

[4] "VHDL code for a VGA driver and for the Test code for the driver", Viewed 04 July 2012, from

http://www.ece.ualberta.ca/~elliott/ee552/studentAppNotes/1998_w/Altera_UP1_Board_Map/vga.html.

[5] Reference manual, "VGA Reference Component", Digilent Romania, March 28, 2008, viewed 5 January 2013, from http://studenter.miun.se/~amiyou/VHDL/Exercises/VGA%20RefComp/VgaRefComp.pdf.

[6] A data sheet, "LM35 Precision Centigrade Temperature Sensors", National Semiconductor Corporation, November 2000, DS005516.

[7] Reference manual, "Digilent Nexys2 Board", Digilent Inc., 215 E Main Suite D | Pullman, WA 99163, July 11, 2011, Doc: 502-134.

P.K. Gaikwad born in Maharashtra, INDIA, on August 29th, 1976, is M.Sc. in Electronic Science, from Department of Electronic Science, University of Pune, Pune (1999), Ph.D. in Electronics, from Shivaji University, Kolhapur (2010), Diploma in VLSI Design, from Silicon Magic Tech. Pune (2000), Diploma in Cyber Laws, from Asian School of Cyber Laws, Pune, Maharashtra, INDIA.

He is Head of the Department, and Assistant Professor in Electronics at Willingdon College, Sangli, Maharashtra, INDIA, and he is in teaching profession since last 13 years. He is working as a Research Guide in Electronics for Shivaji University, Kolhapur. At present three Ph.D. students are working under his guidance. He has published eight research papers at International level Journals and Five papers at National level Journals. He is a co-author of a book: "Harnessing VLSI System Design with EDA Tools", Dordrecht Heidelberg London New York, Springer, 2011. His working platform and area of research interest is the development of Embedded and VLSI based systems; especially which are applicable in Biomedical instrumentation, such as Electrocardiography (ECG), Electroencephalography (EEG).

Dr. P.K. Gaikwad is a member of Board of Studies in Electronics and Departmental Research Committee (DRC) in Electronics as well as Computer Science in Shivaji University, Kolhapur, INDIA.